SMH Technologies®

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Driver v. 5.07

Moreno Ortolan

Interfacing FlashRunner 2.0 with NXP LPC

SMH Technologies S.r.l.

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NXP LPC Series

Supported LPC series by FlashRunner LPC driver are:

LPC800 Series: Low-Cost Microcontrollers (MCUs) based on Arm® Cortex®-M0+ Cores.

The LPC800 series offers a range of low-power, space efficient, low-pin-count options for basic microcontroller applications.
The LPC800 series MCUs, part of the EdgeVerse™ edge computing platform, include differentiated product features, such as an NFC communication interface, mutual capacitive touch, switch matrix for flexible configuration of each I/O pin function and SCTimer/PWM, giving embedded developers unprecedented design-flexibility.

LPC1100 Series: Scalable Entry-level Microcontrollers (MCUs) based on Arm® Cortex®-M0+/M0 Cores.

The LPC1100 series of MCUs deliver advanced power efficiency, a broad selection of package options and a scalable portfolio with connectivity including USB, LCD and CAN interfaces.
In addition, some products include features such as 12-channel/12-bit analog-to-digital converters (ADC), or an I/O handler (IOH), which gives developers added functionality during the design cycle.
LPC1100 series MCUs are ideal for applications prioritizing small size, low pin count and low power consumption with integrated connectivity (USB or CAN) requirements paired with analog, segment LCD or EEPROM.

LPC1200 Series: Robust and Reliable Microcontrollers (MCUs) based on Arm® Cortex®-M0 Cores.

LPC1200 series MCUs run at speeds up to 45 MHz.
They include configurable peripherals such as a windowed watchdog timer (WWDT), programmable digital filter on all GPIO pins for finer control of signal integrity and on-chip ADC.

LPC1300 Series: Entry-level Microcontrollers (MCUs) based on Arm® Cortex®-M3 Cores.

The LPC1300 series offers entry-level MCUs running at speeds up to 72 MHz.
They deliver a high level of performance with low power consumption. With full-speed USB 2.0 including on-chip PHY and ROM drivers and a configurable analog system including a 12-bit ADC, the LPC1300 MCUs are a design upgrade from our pin-compatible LPC1100 series.

LPC1500 Series: Motion Control Microcontrollers (MCUs) based on Arm® Cortex®-M3 Cores.

The LPC1500 series of 32-bit microcontrollers support high-accuracy sensor and sensor less motor control, enabling simultaneous control of multiple motors in highly flexible configurations.
LPC1500 MCUs simplify evaluation and development without requiring deep motor control experience.

LPC1700 Series: Scalable Mainstream Microcontrollers (MCUs) based on Arm® Cortex®-M3 Cores.

LPC1700 series MCUs provide solid mid-range performance and power efficiency.
They support multiple high-bandwidth data streams running simultaneously from peripherals such as Ethernet, USB (host or device), CAN or LCD displays.

LPC1800 Series: High-Performance Microcontrollers (MCUs) based on Arm® Cortex®-M3 Cores.

At 180 MHz, LPC1800 series MCUs combine the industry's fastest Arm® Cortex®-M3 core with multiple high-speed connectivity options, advanced timers, analog and optional security features to secure code and data communications.
All LPC18xx families include flash and flashless options and support large, flexible internal and external memory configurations.

LPC4300 Series: High-Performance Microcontrollers (MCUs) based on Arm® Cortex®-M4/M0 Cores.

LPC4300 Series MCUs combine the high performance and flexibility of an asymmetric dual-core architecture with multiple high-speed connectivity options, advanced timers, analog and optional security features to secure code and data communications.
DSP capabilities enable all LPC43xx families to support complex algorithms in a data-intensive application.
Flash and flashless options support large, flexible internal and external memory configurations.

LPC5500 Series: Arm® Cortex®-M33 based Microcontroller Series for Mass Market, Leveraging 40nm Embedded Flash Technology.

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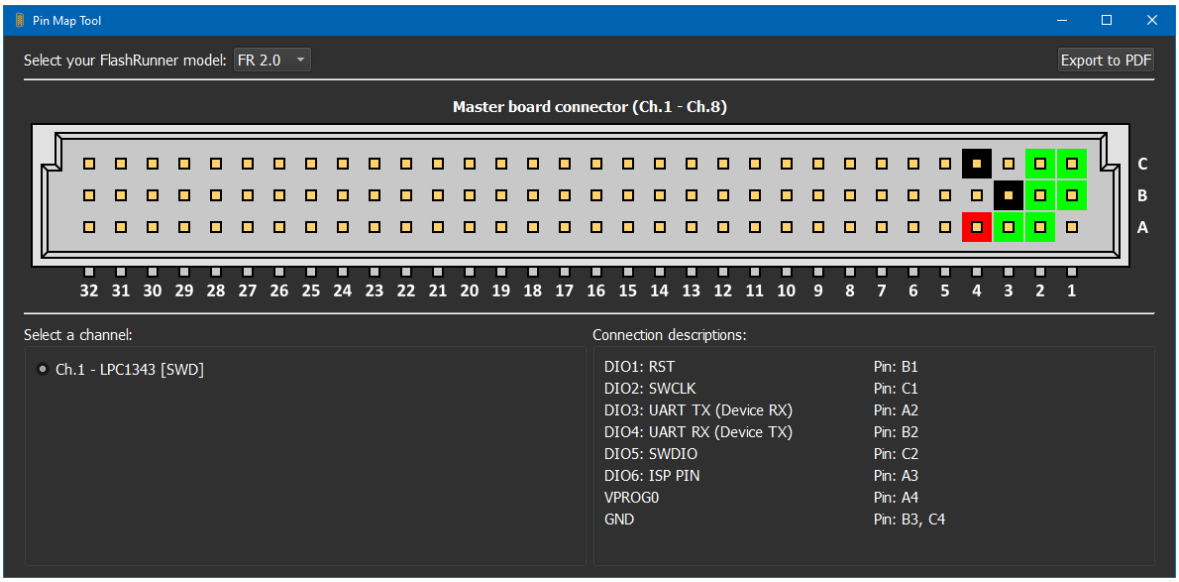
The LPC5500 MCU series leverages Arm's most recent Cortex-M33 technology, combining significant product architecture enhancements and greater integration over previous generations, with dramatic power consumption improvements and advanced security feature including SRAM PUF-based root of trust and provisioning, real-time execution from encrypted images (internal flash), and asset protection with Arm® TrustZone®-M.
In addition, the LPC5500 MCU series features seven scalable families, with a broad package and memory options, as well as a comprehensive MCUXpresso Software and Tools ecosystem and low-cost development boards.
The LPC5500 series of MCUs is part of NXP's EdgeVerse™ edge computing platform.

NXP LPC Protocol and PIN map

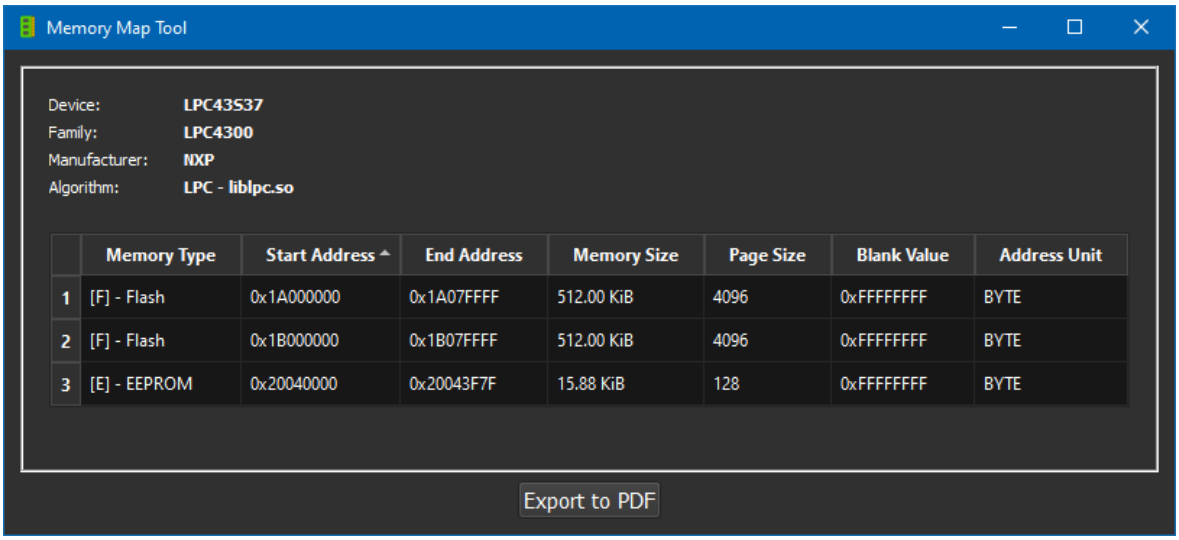
LPC devices support the SWD protocol.

```
#TCSETPAR CMODE <SWD>
```

NXP LPC PIN MAP



NXP LPC Memory Map



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NXP LPC CRP Protection

Available only for LPC800x and LPC1100x series. For other LPC devices please contact SMH Technologies teams.

Code Read Protection is a mechanism that allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the ISP can be restricted.

When needed, CRP is invoked by programming a specific pattern in the flash image at offset 0x000002FC.

NXP LPC CRP Enable Protection

To properly enable CRP protection, we must first know the programming specifications of specific LPC device.

The granularity with which you can write in Flash is 64 | 128 | 256 | 512 | 1024 bytes.
This means that if the Flash is already programmed, it is not possible to write only the CRP value to the address **0x2FC** (4Byte) without touching the other programmed bytes.

The best solution is therefore to patch the FRB file at runtime, and replace the bytes of the FRB file at the address **0x2FC** using dynamic memory.
In this way we will write the CRP value while programming all the FLASH memory.

There are three possible CRP values that can be set:

NXP LPC CRP Level 1

Protection	Pattern at 0x000002FC	Description
CRP1	0x12345678	Access to chip via the SWD pins is disabled. This mode allows partial flash update using the following USART ISP commands and restrictions: • Write to RAM command cannot access RAM below 0x10000380. • Copy RAM to flash command cannot write to Sector 0. • Erase command can erase Sector 0 only when all sectors are selected for erase. • Compare command is disabled. • Read Memory command is disabled. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased. Since compare command is disabled in case of partial updates the secondary loader should implement checksum mechanism to verify the integrity of the flash.

How to enable **CRP 1** with FlashRunner 2.0 Dynamic Memory:

```
#DYNMEMCLEAR
#DYNMEMSET2 0x000002FC 4 78563412
```

NXP LPC CRP Level 2

Protection	Pattern at 0x000002FC	Description
CRP2	0x87654321	Access to chip via the SWD pins is disabled. The following ISP commands are disabled: • Read Memory. • Write to RAM. • Go. • Copy RAM to flash. • Compare. When CRP2 is enabled the ISP erase command only allows erasure of all user sectors.

How to enable **CRP 2** with FlashRunner 2.0 Dynamic Memory:

```
#DYNMEMCLEAR
#DYNMEMSET2 0x000002FC 4 21436587
```


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NXP LPC CRP Level 3

Protection	Pattern at 0x000002FC	Description
CRP3	0x43218765	Access to chip via the SWD pins is disabled. ISP entry selected via the ISP entry pin is disabled if a valid user code is present in flash sector 0. This mode effectively disables ISP override using the entry pin. It is up to the application of the user to provide a flash update mechanism using IAP calls or call reinvoke ISP command to enable flash update via USART. Caution: If CRP3 is selected, no future factory testing can be performed on the device.

How to enable **CRP 3** with FlashRunner 2.0 Dynamic Memory:

```
#DYNMEMCLEAR
#DYNMEMSET2 0x000002FC 4 7073694E
```

NXP LPC CRP NO_ISP

Protection	Pattern at 0x000002FC	Description
NO_ISP	0x4E697370	Prevents sampling of the pins for entering ISP mode. ISP sampling pin is available for other applications.

How to enable **NO_ISP** with FlashRunner 2.0 Dynamic Memory:

```
#DYNMEMCLEAR
#DYNMEMSET2 0x000002FC 4 7073694E
```

NXP LPC Remove CRP protection

The only way to remove the CRP protection is to communicate with the bootloader of the LPC device through **UART** protocol.
For this to happen, the device must boot with the ISP PIN kept low.

So, it is essential to give the FlashRunner access to the **ISP PIN** in DIO6.
At this point the device after a power on or a reset is in ISP mode (UART) so through the **UART TX** and **UART RX** the FlashRunner will remove the CRP protection by deleting the FLASH memory.

At the end of the procedure a power on cycle is required to ensure that the CRP is effectively removed.
Therefore, it is necessary that the device is powered by FlashRunner so that the driver can turn the device off and on at the right time.

After removing the CRP, the driver will return to communicate with the SWD protocol.
Masserase command after remove CRP protection can be skipped because FLASH memory is already erased.

Normally if we connect to a device protected by CRP we get:

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Wrong ID-Code Read. Please check connections or LPC device is protected by CRP level 1, 2 or 3.
080001C4!|.
01|ERR--08001015|FPGA operation timeout.|
```

Instead, if we enable the parameter `#TCSETPAR REMOVE_CRP YES` then the driver will try to remove the CRP protection via UART protocol:

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Attempt to connect via UART protocol (57600bps).
 * Set ISP Pin Low to Enter ISP Mode.
 * Shuffle DIO: shuffling 2->4, 5->3.
 * Reset Device through RESET Pin (DIO1).
 * Received Synchronized frame.
 * Received OK frame for Synchronization.
 * Chip completely Erased.
```


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```
 * Turn OFF and ON target LPC device.
Return to SWD protocol. Reshuffling DIO's.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled
Scanning AP map to find all APs.
AP[0] IDR: 0x04770031, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FF000.
CPUID: 0x410CC601.
Implementer Code: 0x41-[ARM].
Found Cortex M0+ revision r0p1.
Cortex M0+ Core halted [0.001 s].
PLL Enabled.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 6 [Range 4-9].
IDCODE: 0x0BC11477.
Designer: 0x23B, Part Number: 0xBC11, Version: 0x0.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.960 s.
>|
```

NXP LPC Driver Parameters

The standard parameters are used to configure some specific options inside LPC driver.

#TCSETPAR ENTRY_CLOCK

Syntax: `#TCSETPAR ENTRY_CLOCK <Frequency>`

`<Frequency>` Accepted parameters 4000000, 2000000, 1000000, 500000, 100000 Hz

Description: Set the JTAG/SWD frequency used in the Connect procedure before raising the PLL of the device, if the device PLL is available

Note: Default value 4.00 MHz

#TCSETPAR PLL_ENABLED

Syntax: `#TCSETPAR PLL_ENABLED <Value>`

`<Value>` Accepted parameters YES / NO

Description: Enable the PLL of the device at the highest possible frequency if it's available

Note: Default value YES

#TCSETPAR REMOVE_CRP

Syntax: `#TCSETPAR REMOVE_CRP <Value>`

`<Value>` Accepted parameters YES or NO

Description: This command is available from driver version **4.03**
Try to remove CRP protection through UART protocol during Connect procedure

Note: Default value NO

Example: Correct parameter and commands execution: 😊

```
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Attempt to connect via UART protocol (57600bps).
 * Set ISP Pin Low to Enter ISP Mode.
 * Shuffle DIO: shuffling 2->4, 5->3.
```


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```
  * Reset Device through RESET Pin (DIO1).
  * Received Synchronized frame.
  * Received OK frame for Synchronization.
  * Chip completely Erased.
  * Turn OFF and ON target LPC device.
Return to SWD protocol. Reshuffling DIO's.
ID-Code read correctly at 4.00 MHz.
...
Time for Connect: 0.960 s.
>|
```

#TCSETPAR CHECK_SIGNATURE

Syntax: **#TCSETPAR** CHECK_SIGNATURE < Value >

<Value> Accepted parameters YES or NO

Description: Select if you want to check the Flash Signature (Valid User Code) located after eight words into FRB file.
If the Valid User Code is wrong based on previous data into FRB file, a new Valid User Code is automatically calculated and old value is replaced by the new one

Note: This command is available from driver version **5.06**
Default value NO

Example: Correct parameter and commands execution: 😊

```
---#TPCMD PROGRAM F
Valid User Code from FRB: 0xB8F09D93.
Valid User Code calculated: 0x8E263EAF.
Valid User Code from FRB file is not correct. Modified to 0x8E263EAF.
Time for Program F: 0.661 s
>|
---#TPCMD VERIFY F R
Valid User Code from FRB: 0xB8F09D93.
Valid User Code calculated: 0x8E263EAF.
Valid User Code from FRB file is not correct. Modified to 0x8E263EAF.
Time for Verify Readout F: 0.035 s
>|
```

#TCSETPAR RESET_HARDWARE

Syntax: **#TCSETPAR** RESET_HARDWARE <Value>

<Value> Accepted parameters YES / NO

Description: Use Hardware reset (DIO1) into Connect procedure during halt Cortex Core
Please leave this parameter to NO except when it is strictly necessary
Usually, the Software Reset is enough to proceed with the reset of the device and to continue with the programming procedure

Note: Default value NO

#TCSETPAR SAMPLING_POINT

Syntax: **#TCSETPAR** SAMPLING_POINT <Value>

<Value> Accepted values are in the range 1-15

Description: Use this parameter to permanently set the sampling point of the FPGA
It is recommended to leave this parameter with the default value

Note: Default value 17

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NXP LPC Driver Commands

Here you can find the complete list of all available commands for LPC driver.

```
F → Flash
E → EEprom
```

#TPCMD CONNECT

#TPCMD CONNECT

This function performs the entry and is the first command to be executed when starting the communication with the device.

```
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP map detection skipped.
Manually configured AP map found.
Device ready for new AP configuration.
AP port enabled correctly.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FE000.
CPUID: 0x410FD214.
Implementer Code: 0x41-[ARM].
Found Cortex M33 revision r0p4.
Cortex M33 Core halted [0.001 s].
PLL Enabled.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 4-6].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Device configuration:
 * Bootloader version 3.0.0.
 * Flash base 0x00000000.
 * Flash size 0x00010000.
 * Flash block number 1.
 * Flash page size 0x0200.
Time for Connect: 0.116 s.
```

Example of Connect when device is protected by CRP1 or CRP2 protection (with #TCSETPAR REMOVE_CRP YES):

```
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Attempt to connect via UART protocol (57600bps).
 * Set ISP Pin Low to Enter ISP Mode.
 * Shuffle DIO: shuffling 2->4, 5->3.
 * Reset Device through RESET Pin (DIO1).
 * Received Synchronized frame.
 * Received OK frame for Synchronization.
 * Chip completely Erased.
 * Turn OFF and ON target LPC device.
Return to SWD protocol. Reshuffling DIO's.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled
Scanning AP map to find all APs.
AP[0] IDR: 0x04770031, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FF000.
CPUID: 0x410CC601.
Implementer Code: 0x41-[ARM].
Found Cortex M0+ revision r0p1.
Cortex M0+ Core halted [0.001 s].
PLL Enabled.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 6 [Range 4-9].
IDCODE: 0x0BC11477.
Designer: 0x23B, Part Number: 0xBC11, Version: 0x0.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.960 s.
```


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#TPCMD MASSERASE

#TPCMD MASSERASE <F>
This command performs a masserase for Flash memory.

#TPCMD SECTOR_ERASE

#TPCMD SECTOR_ERASE <F>
This command performs a sector erase for all Flash memory.

#TPCMD SECTOR_ERASE <F> <start address> <size>
This command performs a sector erase for selected part of Flash memory.
Enter the Start Address and Size in hexadecimal format.

#TPCMD PAGE_ERASE

#TPCMD PAGE_ERASE <F>
This command performs a page erase for all Flash memory.

#TPCMD PAGE_ERASE <F> <start address> <size>
This command performs a page erase for selected part of Flash memory.
Enter the Start Address and Size in hexadecimal format.

#TPCMD BLANKCHECK

#TPCMD BLANKCHECK <F|E>
Blankcheck is available for Flash and EEprom memory.
Verify if all memory is erased.

#TPCMD BLANKCHECK <F|E> <start address> <size>
Blankcheck is available for Flash and EEprom memory.
Verify if selected part of memory is erased.
Enter the Start Address and Size in hexadecimal format.

#TPCMD PROGRAM

#TPCMD PROGRAM <F|E>
Program is available for Flash and EEprom memory.
Programs all memory of the selected type based on the data in the FRB file.

#TPCMD PROGRAM <F|E> <start address> <size>
Program is available for Flash and EEprom memory.
Programs selected part of memory of the selected type based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY

#TPCMD VERIFY <F|E> <R|S>
R: Readout Mode.
S: Checksum 32 Bit Mode.
Verify Readout/Checksum 32bit is available for Flash and EEprom memory.
Verify all memory of the selected type based on the data in the FRB file.

#TPCMD VERIFY <F|E> <R|S> <start address> <size>
R: Readout Mode.
S: Checksum 32 Bit Mode.
Verify Readout/Checksum 32bit is available for Flash and EEprom memory.

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Verify selected part of memory of the selected type based on the data in the FRB file.
Enter the Start Address and Size in hexadecimal format.

#TPCMD READ

`#TPCMD READ <F|E>`
Read function is available for Flash and EEprom memory.
The result of the read command will be visible into the Terminal.

`#TPCMD READ <F|E> <start address> <size>`
Read function is available for Flash and EEprom memory.
The result of the read command will be visible into the Terminal.
Enter the Start Address and Size in hexadecimal format.

#TPCMD DUMP

`#TPCMD DUMP <F|E>`
Dump function is available for Flash and EEprom memory.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.

`#TPCMD DUMP <F|E> <start address> <size>`
Dump function is available for Flash and EEprom memory.
The result of the dump command will be stored in the FlashRunner 2.0 internal memory.
Enter the Start Address and Size in hexadecimal format.

#TPCMD READ_PART_ID

Syntax: `#TPCMD READ_PART_ID`

Prerequisites: none

Description: This function gets the Part ID from the device

Note: This command prints into Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_PART_ID
Part Identification Number: 0x8041.
Time for Read Part ID: 0.001 s
```

#TPCMD READ_BOOT_CODE_VERSION

Syntax: `#TPCMD READ_BOOT_CODE_VERSION`

Prerequisites: none

Description: This function gets the Boot Code Version from the device

Note: This command prints into Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_BOOT_CODE_VERSION
Boot Code Version Number: 0x0D01.
Time for Read Boot Code Version: 0.001 s
```


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#TPCMD READ_UID

Syntax: `#TPCMD READ_UID`

Prerequisites: none

Description: This function gets the Unique ID UID from the device

Note: This command prints into Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_UID
Read the unique ID:
The 1st 32-bit word: 0x0700D030.
The 2nd 32-bit word: 0xAF2A1CE1.
The 3th 32-bit word: 0x1412031B.
The 4th 32-bit word: 0xF5000703.
Time for Read UID: 0.001 s
```

#TPCMD RUN

Syntax: `#TPCMD RUN <Time [s]>`

<Time [s]>	Time in seconds (i.e., 2 s). This time is an optional parameter.

Prerequisites: none

Description: Move the Reset line up and down quickly if no parameter <Time [s]> is inserted.
`#TPCMD RUN <Time [s]>` instead moves the Reset line down, waits for the entered time and then sets the Reset line high.
This command typically can be used to execute the firmware programmed in the device.

#TPCMD READ_MEM8

Syntax: `#TPCMD READ_MEM8 <Address> <Byte Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<Byte Count>	Byte count in decimal format (i.e., 8 -> eight bytes)

Prerequisites: none

Description: Read memory byte per byte from target LPC device

Note: This command is available from driver version **4.14**
This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM8 0x52002020 8
Read[0x52002020]: 0xF0
Read[0x52002021]: 0xAA
Read[0x52002022]: 0x16
Read[0x52002023]: 0x14
Read[0x52002024]: 0x00
Read[0x52002025]: 0x00
Read[0x52002026]: 0x00
Read[0x52002027]: 0x00
Time for Read Mem: 0.002 s
```


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#TPCMD READ_MEM16

Syntax: `#TPCMD READ_MEM16 <Address> <16-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<16-bit Word Count>	16-bit Word count in decimal format (i.e., 4 -> four 16-bit words)

Prerequisites: none

Description: Read memory 16-bit word per 16-bit word from target LPC device

Note: This command is available from driver version **4.14**
This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM16 0x52002020 4
Read[0x52002020]: 0xAAF0
Read[0x52002022]: 0x1416
Read[0x52002024]: 0x0000
Read[0x52002026]: 0x0000
Time for Read Mem: 0.002 s
```

#TPCMD READ_MEM32

Syntax: `#TPCMD READ_MEM32 <Address> <32-bit Word Count>`

<Address>	Address in HEX format (i.e., 0x52002020)
<32-bit Word Count>	32-bit Word count in decimal format (i.e., 2 -> two 32-bit words)

Prerequisites: none

Description: Read memory 32-bit word per 32-bit word from target LPC device

Note: This command is available from driver version **4.14**
This command prints into Terminal and Real Time Log

Examples: Correct command execution: 😊

```
---#TPCMD READ_MEM32 0x52002020 2
Read[0x52002020]: 0x1416AAF0
Read[0x52002024]: 0x00000000
Time for Read Mem: 0.002 s
```

#TPCMD DISCONNECT

`#TPCMD DISCONNECT`

Disconnect function. Power off and exit.

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NXP LPC Driver Examples

Here you can see a complete example of NXP LPC projects.

1 – NXP LPC LPC5502 64KB example Commands

```
#TCSETPAR ENTRY_CLOCK 4000000
#TCSETPAR PLL_ENABLED YES
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE SWD
#TPSETSRC 64KB.frb
#TPSTART
#TPCMD CONNECT
#TPCMD MASSERASE F
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD DISCONNECT
#TPEND
```

1 – NXP LPC LPC5502 64KB example Real Time Log

```
---#TPSTART
Load SWD FPGA version 0x00001215.
>|
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP map detection skipped.
Manually configured AP map found.
Device ready for new AP configuration.
AP port enabled correctly.
AP[0] IDR: 0x84770001, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FE000.
CPUID: 0x410FD214.
Implementer Code: 0x41-[ARM].
Found Cortex M33 revision r0p4.
Cortex M33 Core halted [0.001 s].
PLL Enabled.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 3 [Range 4-6].
IDCODE: 0x6BA02477.
Designer: 0x23B, Part Number: 0xBA02, Version: 0x6.
ID-Code read correctly at 37.50 MHz.
Device configuration:
 * Bootloader version 3.0.0.
 * Flash base 0x00000000.
 * Flash size 0x00010000.
 * Flash block number 1.
 * Flash page size 0x0200.
Time for Connect: 0.116 s.
>|
---#TPCMD MASSERASE F
Time for Masserase F: 0.003 s
>|
---#TPCMD BLANKCHECK F
Time for Blankcheck F: 0.001 s
>|
---#TPCMD PROGRAM F
```


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```
Time for Program F: 0.187 s
>|
---#TPCMD VERIFY F R
Time for Verify Readout F: 0.087 s
>|
---#TPCMD DISCONNECT
>|
```

1 – NXP LPC LPC5502 64KB example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.116 s
Masserase Flash	0.003 s
Blankcheck Flash	0.001 s
Program Flash	0.187 s
Verify Readout Flash	0.087 s
Cycle Time	**00:00.451 s**

2 – NXP LPC LPC804M101 with CRP enabled example Commands

```
#TCSETPAR PLL_ENABLED YES
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR REMOVE_CRP YES
#TCSETPAR RESET_HARDWARE NO
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE SWD
#TCSETPAR CHECK_SIGNATURE YES
#TPSETSRC LPC804M101.frb
#DYNMEMCLEAR
#DYNMEMSET2 0x000002FC 4 21436587
#TPSTART
#TPCMD CONNECT
#TPCMD MASSERASE F
#TPCMD BLANKCHECK F
#TPCMD PROGRAM F
#TPCMD VERIFY F R
#TPCMD READ_UID
#TPCMD READ_BOOT_CODE_VERSION
#TPCMD READ_PART_ID
#TPCMD DISCONNECT
#TPEND
```

2 – NXP LPC LPC804M101 with CRP enabled example Real Time Log

```
---#TPSTART
Load SWD FPGA version 0x00001215.
>|
---#TPCMD CONNECT
Protocol selected SWD.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
Attempt to connect via UART protocol (57600bps).
 * Set ISP Pin Low to Enter ISP Mode.
 * Shuffle DIO: shuffling 2->4, 5->3.
 * Reset Device through RESET Pin (DIO1).
 * Received Synchronized frame.
 * Received OK frame for Synchronization.
```


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```
 * Chip completely Erased.
 * Turn OFF and ON target LPC device.
Return to SWD protocol. Reshuffling DIO's.
ID-Code read correctly at 4.00 MHz.
JTAG-SWD Debug Port enabled.
Scanning AP map to find all APs.
AP[0] IDR: 0x04770031, Type: AMBA AHB3 bus.
AP[0] ROM table base address 0xE00FF000.
CPUID: 0x410CC601.
Implementer Code: 0x41-[ARM].
Found Cortex M0+ revision r0p1.
Cortex M0+ Core halted [0.001 s].
PLL Enabled.
Requested Clock is 37.50 MHz.
Generated Clock is 37.50 MHz.
Good samples: 4 [Range 4-7].
IDCODE: 0x0BC11477.
Designer: 0x23B, Part Number: 0xBC11, Version: 0x0.
ID-Code read correctly at 37.50 MHz.
Time for Connect: 0.957 s.
>|
---#TPCMD MASSERASE F
Time for Masserase F: 0.625 s
>|
---#TPCMD BLANKCHECK F
Time for Blankcheck F: 0.008 s
>|
---#TPCMD PROGRAM F
CRP Protection will be set to CRP2 after power cycle.
Valid User Code from FRB: 0xB8F09D93.
Valid User Code calculated: 0x8E263EAF.
Valid User Code from FRB file is not correct. Modified to 0x8E263EAF.
Time for Program F: 0.662 s
>|
---#TPCMD VERIFY F R
Valid User Code from FRB: 0xB8F09D93.
Valid User Code calculated: 0x8E263EAF.
Valid User Code from FRB file is not correct. Modified to 0x8E263EAF.
Time for Verify Readout F: 0.035 s
>|
---#TPCMD DISCONNECT
>|
```

2 – NXP LPC LPC804M101 with CRP example Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.957 s
Masserase Flash	0.625 s
Blankcheck Flash	0.008 s
Program Flash	0.662 s
Verify Readout Flash	0.035 s
Cycle Time	**00:02.139 s**

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NXP LPC Driver Changelog

Info about driver versions prior to 4.00
All driver versions prior to 4.00 are to be considered obsolete, please update your driver to the latest version.

Info about driver version 4.00 - 14/02/2021
Supported LPC -> LPC802M001, LPC802M011.

Info about driver version 4.01 - 19/02/2021
Supported LPC -> LPC1769, LPC1768, LPC1767, LPC1766, LPC1765, LPC1764, LPC1763, LPC1759, LPC1758, LPC1756, LPC1754, LPC1752.

Info about driver version 4.02 - 23/02/2021
Supported LPC -> LPC804M101, LPC804M111.

Info about driver version 4.03 - 26/03/2021
Supported LPC Remove CRP protection. Available only for LPC804M101, LPC804M111 devices. Enable this feature with `#TCSETPAR REMOVE_CRP YES`.

Info about driver version 4.04 - 06/04/2021
Supported LPC Remove CRP protection for LPC802xx device. Enable this feature with `#TCSETPAR REMOVE_CRP YES`.

Info about driver version 4.05 - 19/07/2021
Internal update for FPGA name and version tracking.

Info about driver version 4.06 - 28/07/2021
Supported LPC -> LPC822M101, LPC824M201.

Info about driver version 4.07 - 03/08/2021
Upgraded Connect Under Reset Procedure.
Supported LPC -> LPC4312, LPC4313, LPC4315, LPC4317, LPC4322, LPC4323, LPC4325, LPC4327, LPC4333, LPC4337, LPC4353, LPC4357, LPC4367, LPC43S37, LPC43S57, LPC43S67.

Info about driver version 4.08 - 09/08/2021
Supported LPC -> LPC1517, LPC1518, LPC1519, LPC1547, LPC1548, LPC1549.

Info about driver version 4.09 - 11/08/2021
Supported LPC -> LPC5502, LPC5504, LPC5506, LPC55S04, LPC55S06.

Info about driver version 4.10 - 12/08/2021
Internal upgrade of the algorithm, no change to the operations it performs.

Info about driver version 4.11 - 30/08/2021
Connection procedure updated, now LPC driver automatically find the best entry sequence.

Info about driver version 4.12 - 21/09/2021
Connection procedure updated to handle special cases.

Info about driver version 4.13 - 04/11/2021
Internal update, upgraded management for reset FPGA procedure.

Info about driver version 4.14 - 25/01/2022
Added `#TPCMD READ_MEM8`, `#TPCMD READ_MEM16`, `#TPCMD READ_MEM32` commands.

Info about driver version 4.15 - 26/01/2022
Upgraded WWDT clock and interrupts management for LPC55x series.

Info about driver version 4.16 - 14/03/2022
Internal upgrade of the algorithm, no change to the operations it performs.

Info about driver version 4.17 - 05/04/2022
Upgraded Remove CRP procedure for LPC804xx.

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Info about driver version 4.18 - 16/06/2022
Print current FPGA version loaded into TPSTART command.
Upgraded internal code to align all drivers.

Info about driver version 4.19 - 21/06/2022
Added full support of LPC1100 series.
Added full support of LPC1200 series.
Added full support of LPC1300 series.
Completed support of LPC1700 series.

Info about driver version 4.20 - 29/06/2022
Added full support of LPC1800 series.

Info about driver version 4.21 - 30/06/2022
Added full support of LPC800 series.

Info about driver version 5.00 - 28/07/2022
Added FPGA for new FlashRunner 2.0 models.

Info about driver version 5.01 - 01/12/2022
Supported Remove CRP protection for LPC1100x series.

Info about driver version 5.02 - 12/12/2022
Supported LPC11E35x401 and LPC11E37x401 devices.

Info about driver version 5.03 - 04/01/2023
Implemented Halt Cortex Core M33 with Software Breakpoint when we need to halt immediately customer firmware execution.

Info about driver version 5.04 - 05/01/2023
Upgraded connect procedure for LPC55x series.

Info about driver version 5.05 - 09/06/2023
Supported LPC552x, LPC55S2x and LPC55S6x series.

Info about driver version 5.06 - 07/09/2023
Added `#TCSETPAR CHECK_SIGNATURE` to check the Flash Signature and modify it if there is a wrong value into FRB file.

Info about driver version 5.07 - 09/11/2023
Supported LPC860x series.

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